Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A method for processing packet information using an array of processing elements comprising:

performing a first search using a first stage processing element related to a packet using first search information;

performing, in parallel with the first search, search-independent processing using a second stage processing element on information related to the packet; and

performing search-dependent processing using a result from the first search and a result of the search-independent processing to produce second search information.

2. (original) The method of claim 1 further including performing a second search using the second search information.

3. (original) The method of claim 2 further including holding a processing state from the search-independent processing until the result from the first search is available.

4. (original) The method of claim 2 wherein performing search-dependent processing to produce the second search information includes producing a comparand and a mask as the second search information.

5. (original) The method of claim 4 wherein performing the second search includes searching a content addressable memory using the comparand and the mask.

6. (previously presented) A method for processing packet information comprising:

processing information related to a packet using a first stage processing element to produce a first search key, wherein the first stage processing element is included within an array of processing elements;

searching a first stage memory unit using the first search key;

performing, in parallel with the search of the first stage memory unit, search-independent processing on information related to the packet using a second stage processing element, wherein the second stage processing element is included within the array of processing elements;

performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key; and

searching a second stage memory unit using the second search key.

7. (original) The method of claim 6 further including holding a processing state from the search-independent processing until the result from the search of the first stage memory unit is received at the second stage processing element.

8. (original) The method of claim 7 further including providing the result from the search of the first stage memory unit directly to the second stage processing element from the first stage memory unit.

9. (original) The method of claim 6 further including providing the result from the search of the first stage memory unit directly to the second stage processing element from the first stage memory unit.

10. (original) The method of claim 6 wherein the first and second search keys include a comparand and a mask.

11. (original) The method of claim 6 further including forwarding information related to the packet to the second stage processing element before the result from the search of the first stage memory is produced.

12. (original) A system for processing packet information comprising:

an array of processing elements having;

at least one first stage processing element; and

at least one second stage processing element; and

a first stage memory unit that is searched in response to search information from the first stage processing element;

wherein the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet.

13. (original) The system of claim 12 further including a direct communications link between the first stage memory unit and the second stage processing element configured to provide search results directly to the second stage processing element from the first stage memory unit.

14. (original) The system of claim 12 wherein the second stage processing element is further configured to perform search-dependent processing using a result of the search of the first stage memory unit and a result from the search-independent processing to produce a search key.

15. (original) The system of claim 14 further including a second stage memory unit that is associated with the second stage processing element, wherein the search key is used to search the second stage memory unit.

16. (original) The system of claim 15 further including at least one third stage processing element, wherein the second and third stage processing elements are

configured to allow the third stage processing element to perform search-independent processing related to the packet in parallel with the search of the second stage memory unit.

17. (original) The system of claim 12 wherein the first stage memory unit comprises content addressable memory.

18. (previously presented) A system for processing packet information comprising:

an array of processing elements having;

a plurality of first stage processing elements; and

a plurality of second stage processing elements; and

a memory interface that is configured to provide search information to a first stage memory unit from the plurality of first stage processing elements and to provide search results from the first stage memory unit directly to the plurality of second stage processing elements, wherein the first and second stage processing elements are configured to allow the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit, where the searches are related to the same packets.

19. (canceled)

20. (original) The system of claim 18 wherein the first stage processing elements forward information to respective second stage processing elements before results from respective searches of the first stage memory unit are received by the second stage processing elements.

21. (original) The system of claim 18 further including:

a first bus that connects the plurality of first stage processing elements to the memory interface; and

a second bus that connects the plurality of second stage processing elements to the memory interface.